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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,510	11/27/2001	Kenneth Y. Chiu	5181-95300	2233

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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,510	CHIU, KENNETH Y.	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/02,7/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 3 July 2003 was filed after the mailing date of 27 November 2001 for application 09/996,510. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

The information disclosure statement (IDS) submitted on 22 April 2002 was filed after the mailing date of 27 November 2001 for application 09/996,510. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Khanna et al (U.S. 6,539,455).

As per independent claim 1, Khanna et al teach,

- receiving a transfer request corresponding to a block of data, wherein said block comprises a plurality of sub-blocks; (Column 22 lines 37-43). *The Examiner notes that Khanna et al teach of "loading" the CAM devices. The "loading" is acted upon by a "compare instruction" which the Examiner*

notes is a request that will produce a result that can then be transferred to the system issuing the "compare instruction." Accordingly, the "compare instruction", as taught by Khanna et al, is the transfer request as disclosed in the instant limitation.

- generating an address corresponding to each of said sub-blocks; detecting which of said sub-blocks are required as part of said transfer request; and utilizing only those generated addresses which correspond to the sub-blocks which are required. (Column 22 line 66 to Column 23 line 5). *The Examiner notes that the system of Khanna et al completes the "compare instruction" as discussed supra, and with respect to the instant limitations, the system then proceeds to "output the match index of the location in its CAM array." The "location" will contain an address in memory that corresponds to the matched entry of the "compare instruction". Accordingly, each individual entry, whether matching the "compare instruction" or not, will have an address generated that corresponds to its individual location in memory.*

As per dependent claim 2, Khanna et al teach, "further comprising receiving a mask which corresponds to the request, wherein the mask indicates which of said sub-blocks are required as part of the request, and wherein detecting which of said sub-blocks are required comprises examining said mask" (Column 17 lines 45-55). *The Examiner notes that Khanna et al teach of "prefix mask data" that is relied upon to indicate whether the data in a specific memory cell should be masked. Accordingly, the*

mask as disclosed in the instant claim is contained within the "prefix mask data" as taught by Khanna et al.

As per dependent claim 3, Khanna et al teach, "wherein said mask comprises a bit corresponding to each of said sub-blocks, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required" (Column 17 lines 45-55). *As discussed supra, with respect to the "prefix mask data", a determination is made as to whether or not the system will rely on the data in a specific memory cell. Accordingly, the Examiner further notes that the "prefix mask data" must include a bit, or logic 'high' or 'low', that communicates to the system whether the sub-block is required or not.*

As per dependent claim 4, Khanna et al teach, "wherein said request includes an address corresponding to said block, and wherein said transfer comprises transferring one of said sub-blocks at a time" (Column 22 lines 37-43).

As per dependent claim 5, Khanna et al teach, "wherein each of said addresses corresponding to said sub-blocks are generated concurrently" (Column 22 lines 37-43). *The Examiner notes that as discussed supra, addresses will be generated based upon the "compare instruction". If there are two matches, then the addresses will be generated at the same time based upon the instruction. Accordingly, the addresses will be 'generated concurrently.'*

As per dependent claim 6, Khanna et al teach, "wherein said detecting comprises: detecting a first bit of said mask which has a first value, wherein said first bit

corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block" (Column 17 lines 45-55).

As per dependent claim 7, Khanna et al teach, "wherein said detecting further comprises: masking off said first bit of said mask, subsequent to utilizing said first address; detecting a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and selecting a second address of said generated addresses which corresponds to the second sub-block" (Column 17 lines 45-55).

As per dependent claim 8, Khanna et al teach, "determining a first number of said sub-blocks are required; and detecting transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred" (Column 22 line 66 to Column 23 line 5). *The Examiner notes that as discussed supra, matches from the "compare instruction" will be generated and passed on. In order for the system to maintain accurate results, an equal number of matches that are detected must be passed on (transferred) back to the system of Khanna et al to further select the best match.*

As per independent claim 9, the Examiner notes that in addition to the limitations as discussed supra with respect to independent claim 1, the instant claim further recites a first interface and a second interface embodied on a device. Khana et al teaches a first interface as "mask cells" (see column 5 lines 9-10) and a second interface as a "CAM match line" (see column 5 lines 8-12).

As per dependent claim 10, Khanna et al teach, "wherein said first interface is further configured to receive a mask corresponding to the request, wherein the mask indicates which of said sub-blocks are required as part of the request, and wherein said second interface is further configured to detect which of said sub-blocks are required by examining said mask" (Column 17 lines 45-55). *The Examiner notes that Khanna et al teach of "prefix mask data" that is relied upon to indicate whether the data in a specific memory cell should be masked. Accordingly, the mask as disclosed in the instant claim is contained within the "prefix mask data" as taught by Khanna et al.*

As per dependent claim 11, Khanna et al teach, "wherein said mask comprises a bit corresponding to each of said sub-blocks, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required" (Column 17 lines 45-55). *As discussed supra, with respect to the "prefix mask data", a determination is made as to whether or not the system will rely on the data in a specific memory cell. Accordingly, the Examiner further notes that the "prefix mask data" must include a bit, or logic 'high' or 'low', that communicates to the system whether the sub-block is required or not.*

As per dependent claim 12, Khanna et al teach, "wherein said request includes an address corresponding to said block, and wherein said second interface is configured to initiate transfer of only one of said sub-blocks at a time" (Column 22 lines 37-43).

As per dependent claim 13, Khanna et al teach, "wherein said second interface is configured to generate each of said addresses corresponding to said sub-blocks

concurrently" (Column 22 lines 37-43). *The Examiner notes that as discussed supra, addresses will be generated based upon the "compare instruction". If there are two matches, then the addresses will be generated at the same time based upon the instruction. Accordingly, the addresses will be 'generated concurrently.'*

As per dependent claim 14, Khanna et al teach, "wherein said second interface is configured to detect which of said sub-blocks are required by: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block" (Column 17 lines 45-55).

As per dependent claim 15, Khanna et al teach, "wherein said second interface is further configured to detect said required sub-blocks by: masking off said first bit of said mask, subsequent to utilizing said first address; detecting a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and selecting a second address of said generated addresses which corresponds to the second sub-block" (Column 17 lines 45-55).

As per dependent claim 16, Khanna et al teach, "wherein said second interface is further configured to: determine a first number of said sub-blocks are required; and detect transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred" (Column 22 line 66 to Column 23 line 5). *The Examiner notes that as discussed supra, matches from the "compare instruction" will be generated and passed on. In order for the system to maintain accurate results, an equal number of matches that are detected must be*

passed on (transferred) back to the system of Khanna et al to further select the best match.

As per independent claim 17, Khanna et al teach,

- a control unit, wherein said control unit is configured to control access to a plurality of blocks of data, wherein each of said blocks of data comprise a plurality of sub-blocks, and wherein said control unit is not configured to convey a full block of said blocks of data at one time; (Column 5 lines 9-10) *The Examiner notes that the CAM cells are connected via a bus as shown in Figure 8A items 806 and 812. The Examiner further notes that in all computing systems, the memory cells are connected to a controller or processor. Accordingly, the 'control unit' as found in the instant claim is the controller or processor to which the memory cells are connected to via said bus.*
- a first interface coupled to said control unit, wherein said interface is configured to: (Column 5 lines 9-10)
- receive a transfer request, wherein said request corresponds to a first block of said blocks of data; (Column 22 lines 37-43). *The Examiner notes that Khanna et al teach of "loading" the CAM devices. The "loading" is acted upon by a "compare instruction" which the Examiner notes is a request that will produce a result that can then be transferred to the system issuing the "compare instruction." Accordingly, the "compare*

instruction", as taught by Khanna et al, is the transfer request as disclosed in the instant limitation.

- generate an address corresponding to each sub-block of said first block; detect which of said sub-blocks are required as part of said transfer request; and utilize only those generated addresses which correspond to the sub-blocks which are required. (Column 22 line 66 to Column 23 line 5). *The Examiner notes that the system of Khanna et al completes the "compare instruction" as discussed supra, and with respect to the instant limitations, the system then proceeds to "output the match index of the location in its CAM array." The "location" will contain an address in memory that corresponds to the matched entry of the "compare instruction". Accordingly, each individual entry, whether matching the "compare instruction" or not, will have an address generated that corresponds to its individual location in memory.*

As per dependent claim 18, Khanna et al teach," wherein said first interface is further configured to: receive a mask corresponding to said request, wherein the mask indicates which of said sub-blocks are required as part of the request; and detect which of said sub-blocks are required by examining said mask" (Column 17 lines 45-55). *The Examiner notes that Khanna et al teach of "prefix mask data" that is relied upon to indicate whether the data in a specific memory cell should be masked. Accordingly, the mask as disclosed in the instant claim is contained within the "prefix mask data" as taught by Khanna et al.*

As per dependent claim 19, Khanna et al teach, "wherein said mask comprises a plurality of bits, each of which correspond to a sub-block of said first block, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required" (Column 17 lines 45-55). *As discussed supra, with respect to the "prefix mask data", a determination is made as to whether or not the system will rely on the data in a specific memory cell. Accordingly, the Examiner further notes that the "prefix mask data" must include a bit, or logic 'high' or 'low', that communicates to the system whether the sub-block is required or not.*

As per dependent claim 20, Khanna et al teach, "wherein said first interface is configured to generate each of said addresses corresponding to said sub-blocks concurrently" (Column 22 lines 37-43). *The Examiner notes that as discussed supra, addresses will be generated based upon the "compare instruction". If there are two matches, then the addresses will be generated at the same time based upon the instruction. Accordingly, the addresses will be 'generated concurrently.'*

As per dependent claim 21, Khanna et al teach, "wherein said first interface is configured to detect which of said sub-blocks are required by: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block" (Column 17 lines 45-55).

As per dependent claim 22, Khanna et al teach, "wherein said first interface is further configured to: mask off said first bit of said mask, subsequent to utilizing said first

address; detect a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and select a second address of said generated addresses which corresponds to the second sub-block" (Column 17 lines 45-55).

As per dependent claim 23, Khanna et al teach, "wherein said first interface is further configured to: determine a first number of said sub-blocks are required; and detect transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred" (Column 22 line 66 to Column 23 line 5). *The Examiner notes that as discussed supra, matches from the "compare instruction" will be generated and passed on. In order for the system to maintain accurate results, an equal number of matches that are detected must be passed on (transferred) back to the system of Khanna et al to further select the best match.*

Conclusion

The prior art made of record and not relied upon are as follows:

1. U.S. Patent No. 6,622,208 North teaches a comparison routine.
2. U.S. Patent No. 6,591,331 Khanna teaches a method of determining an address.
3. U.S. Patent No. 6,502,163 Ramankutty teaches a CAM update method without a reordering of entries.
4. U.S. Patent No. 6,307,855 Hariguchi teaches a masking lookup method.
5. U.S. Patent No. 6,256,722 Acton et al teach a method of transferring data.
6. U.S. Patent Application Publication 2001/0005876 Srinivasan et al teach a synchronous CAM.

7. U.S. Patent No. 5,893,137 Parks et al teach a matching routine for CAM.

8. U.S. Patent No. 5,696,941 Jung teaches a lookup table method for converting data.

9. U.S. Patent No. 5,490,264 Wells et al teach a mapping method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CPC/mb MB

CHRISTIAN CHACE
PRIMARY EXAMINER